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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,163	07/28/2003	S. Jauher A. Zaidi	63479.0118	4353

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EXAMINER	
MYERS, PAUL R	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 09/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,163	ZAIDI ET AL.	
	Examiner	Art Unit	
	Paul R. Myers	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/28/03*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 6, 9-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims which combines description of the single semiconductor integrated circuit with description of method of making/using it violates 35 U.S.C. 112, since the purpose of that paragraph is to require patentee to provide others with notice of boundaries of protection provided by the patent, since a manufacturer or seller at time of making or selling the structure set forth in the claim would have no indication whether it might later be sued for contributory infringement if the structure is later used in accordance with the claimed method. *Ex parte Lyell* 17 USPQ2d 1548.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 6, 9-14 are rejected under 35 U.S.C. 101 because claims which are intended to embrace both product or machine and process is precluded by language of 35 U.S.C. 101, which sets forth statutory classes of invention in alternative only, and is also invalid under 35 U.S.C. 112, second paragraph, since claim which purports to be both machine and process is ambiguous and therefore does not particularly point out and distinctly claim the subject matter of the invention. *Ex parte Lyell* 17 USPQ2d 1548.

Claims 9-14 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

While "A dependent claim" may be useful and have monetary value "a dependent claim" is not one of the statutory classes of invention set forth under 35 U.S.C. 101.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-9, 11-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lambrecht et al PN 5,935,232 in view of Elabd PN 6,526,462 and Geiger et al PN 4,672,587.

In regards to claims 1, 3, 5, 7: Lambrecht et al teaches A System-on-chip (SOC) apparatus (100), comprising: a single semiconductor integrated circuit that includes one or more processor subsystems (modules 210 Column 9 lines 17-25); a first internal unidirectional bus that

couples to said one or more processor subsystems Figure 2 bus 232 or 230 or alternatively Figure 3 bus 332 or 330), said first internal unidirectional bus has a clock signal and controls transactions between said one or more processor subsystems (Clock Column 2 lines 14-15). Lambrecht et al states the modules 210 can be controllers, memories and application specific integrated circuits however Lambrecht et al does not expressly state the modules include DMA peripherals and memory access controllers. Lambrecht et al does not teach pipelined memory transactions including out-of-order transactions. Lambrecht et al also does not teach a centralized address decoder. Elabd teaches a system on a chip that includes a DMA peripheral (6), memory access controller (30), and pipelined memory transactions including out-of-order transactions (Column 7 line 64 to Column 8 line 14 and Column 9 line 25 to Column 10 line 16) It would have been obvious to include Elabd's memory management in the system of Lambrecht et al because this would have increased data processing throughput. Geiger et al teaches centralized address decoding (Figure 4 item 3') It would have been obvious to include centralized address decoding because this would have prevented having to repeat multiple decoders thus saving chip space.

In regards to claims 2, 4, 6, 8: Lambrecht et al teaches non-DMA peripherals such as memories and ASIC's a second internal unidirectional bus (230 or 330) that couples said one or more processor subsystems via an interface controller (220) to said non-DMA peripherals, said second internal unidirectional bus has a clock signal (clock) and controls transactions between said one or more processor subsystems, and said non-DMA peripherals) using unidirectional address and transaction control signals.

In regards to claims 9, 15-18 dependant upon any of claims 1-4: Lambrecht et al teaches said single semiconductor integrated circuit further includes a bus arbiter (350 Column 6 lines 23-30) coupled to said first internal unidirectional bus (332), wherein said arbiter grants access to said first internal unidirectional bus and arbitrates memory accesses for transactions on said first internal unidirectional bus.

In regards to claim 11: Elabd teaches handling Burst read and writes.

In regards to claim 12: Elabd teaches a variable number of clock cycles between pipelined memory transactions (Column 13 line 63 to Column 14 line 8).

In regards to claims 13-14: Lambrecht et al teaches different clock rates on the different buses.

6. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lambrecht et al PN 5,935,232 in view of Elabd PN 6,526,462 and Geiger et al PN 4,672,587 as applied to claim 9 above, and further in view of Qureshi et al PN 6,353,867.

In regards to claim 10: Lambrecht et al teaches requests that can be received in any order. Lambrecht et al does not expressly teach memory access arbitration for a selected transaction either overlaps a data transfer associated with a prior transaction. Qureshi et al teaches a System On a Chip that handles on chip split transactions which are memory transactions that overlaps a data transfer associated with prior transactions. It would have been obvious to handle split transactions because this would have prevented waiting of memory accesses that art not ready.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul R. Myers whose telephone number is 703 305 9656. The examiner can normally be reached on Mon-Thur 6:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703 305 4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul R. Myers

PRM
September 8, 2004

PAUL R. MYERS
PRIMARY EXAMINER